IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology
Vol. 3, Issue 1, January 2016

Design and Analysis of Resistorless Analog to Digital Converter using CMOS Technology

Chaitali D. Gulhane[1], P. R. Gumble[2]

P.G. Student, Electronics & Telecommunication Dept., Sipna College of Engineering & Technology, Amravati, India[1]

Professor, Electronics & Telecommunication Dept., Sipna College of Engineering & Technology, Amravati, India[2]

Abstract: Generally real time signals are analog in nature. For any type of applications such as in signal processing we require digital signals for processing so to convert the analog signals into digital "Analog to digital converter" is used. Nowadays for reducing chip size area designers searching analog to digital converter architectures using CMOS techniques. The performance of any digital system is depends on the performance parameter of analog to digital converter. In the basic ADC structure, resistors are used for generating the reference voltages at the comparator. So here we will design three resistorless circuits which reduces the power demand of an Analog to Digital Converter are 1) Switched Inverter Scheme (SIS) ADC 2) Clocked Switched Inverter Scheme ADC 3) Sleep transistor switched inverter scheme ADC. This paper presents design and resistorless Analog to Digital Converter with different comparators using CMOS transistors only. It improves efficiency, reduces chip area and also will operating on low power. Finally analysis of Analog to Digital Converters with different comparators will be made to achieve best efficient of Analog to Digital Converter among others.

Keywords: Analog to digital converter, low power, resistorless, switched inverter scheme (SIS) Comparator.

I. INTRODUCTION

Analog-to-digital converters (ADCs) are main design blocks in modern digital communication systems. The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word .The performance parameters of ADC are resolution, quantization error, conversion time. There are various types of ADCs using various techniques which are single ramp ADC, ADC using DAC, Flash ADC.

The proposed work will concentrate on the parameters like power consumption, chip area and efficiency. Analysis will be done with A to D converter using SIS, clocked SIS , SIS comparator with sleep transistor types.

II. LITERATURE REVIEW

Flash ADC Comparators and Techniques for Their Evaluation" proposed Flash ADC comparators and technique.

In this paper they designed three flavors of a periodic comparator to minimize its phase-dependent nonlinearities. One flavor used a differential "quasi-one-junction" SQUID (DQOS) quantizer with a low-inductance clocking scheme. The second flavor used a differential SQUID wheel quantizer, and the third flavor used a symmetric differential SQUID wheel quantizer with time interleaved clocks. They also described a different common mode biasing scheme that gates the quantized signal to apply full signal during the clock aperture, and an attenuated signal outside the clock aperture. They also developed a new performance analysis scheme based on sweeping the dc offset of a single periodic comparator during beat frequency test while following the position of its threshold, which yield both signal reconstruction and duty cycle of the comparator. Using this, they discovered the dependence of the sensitivity of the comparator duty cycle to its dc bias and the slew rate of the signal.[1]

"4-Bit Flash Analog to Digital Converter Design using CMOS-LTE Comparator" proposed 4-bit, 1.8V Flash Analog to Digital Converter (ADC) design using CMOS-LTE (CMOS Linear Tunable Transcoductance Element) Comparator with 500nm technology. In their work they used reference voltages were generated by systematically sizing the transistors of the comparators, thus completely eliminating the resistive ladder network required for the architecture. They designed and simulated TIQ Comparator Flash ADC and CMOS-LTE Comparator Flash ADC with 500 nm technology.[2]

"New Flash ADC Scheme With Maximal 13 Bit Variable Resolution and Reduced Clipped Noise for High-Performance Imaging Sensor" proposed flash ADC with 13 bit variable resolution. In their work they presented a high-performance complementary metal–oxide–semiconductor (CMOS) imager with a new analog-to-digital-converter (ADC) scheme.

The new ADC scheme, adopting the visual perception of human eyes, has realized a maximal 13 bit variable resolution and reduced clipped noise for imaging. This ADC architecture used an adjustable reference at both the top and bottom of the series of nonuniform resistors to reduce the clipped noise and to provide a wide dynamic range to image sensors. The sensors with the newly developed ADC scheme are fabricated by the 0.18-µm CMOS process. The test results show improved image quality compared to typical CMOS products with a linear ADC. Test results also showed 79-dB signal-to-noise ratio (at gain = 0 dB) with a power consumption of 90 mW at 54 MHz. [3]

IARJSET
ISSN (Online) 2393-8021
ISSN (Print) 2394-1588
International Advanced Research Journal in Science, Engineering and Technology
Vol. 3, Issue 1, January 2016

"55- mw 300-MHz Analog – Digital Converters using Digital VLSI technology" proposed Analog to Digital Converter using Digital VLSI technology . In their work they presented two versions of ADC that is selected transistors in comparator were designed with channel length of 1.6 micron in one version and 1.2 micron in another. In their final work they shows the statistical difference in DNL between these two versions of ADC designs at 3 sampling frequencies from 30 chips (1920comparators). The additional 0.4 micron channel length slightly improves the differential non-linearity at lower sampling frequency, and the improvement is more pronounce at higher frequencies. The probability that the DNL is less than 0.5 is 90 %.[4]

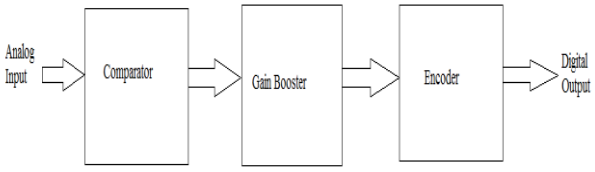
"Design of Analog to Digital Converter Using CMOS Logic" proposed Analog to Digital Converter Using CMOS technology .In their work they designed a 3-bit flash ADC using Threshold Inverter Quantization technique with 130nm CMOS technology for high speed and low voltage applications. Threshold Inverter Quantization (TIQ) is a unique way to generate a comparator for a high speed CMOS flash ADC. They improved the fat tree encoder that is highly suitable for the ultrahigh speed flash ADCs. The fat tree encoder was an effective solution for the bottleneck problem in ultra-high speed ADCs. The proposed A/D converter was suitable for System on Chip (SoC) applications in wireless products and other ultra-high speed applications.[5]

III.PROPOSED WORK

We are going to use three types of comparators .These are

1) Switched Inverter Scheme (SIS) Comparator.
2) Clocked SIS comparator
3) SIS comparator with sleep transistor.

The basic block diagram of proposed ADC is



The basic blocks of Analog to Digital Converter are comparator and encoder. An analog signal is given to the comparator which compares reference voltage with the analog input voltage. The output of comparator is connected to an input of encoder. The encoder is sampled by a pulse on the enable input and a binary code representing the analog input appears on encoder output.

1)Switched Inverter Scheme (SIS) Comparator

When focusing on overall power for an ADC, the power dissipation of the comparator is important contributor. In case of n bit flash converters the number of comparator equals 2n-1.The switched inverter scheme (SIS) also called Threshold inverter quantization (TIQ) comparator has very simple architecture. It is quite different than the conventional operational amplifier based differential input voltage (DIV) comparator. In SIS for n-bit ADC, reference voltage for each comparator is generated by varying transistor size. The SIS comparator design consists of two pairs of inverters connected back to back. Each of the inverter is sized separately to get a unique switching voltage. The cascaded inverters then work as voltage comparator. The full scale voltage range (VFSR) is equally divided by 2n-1 SIS comparators.

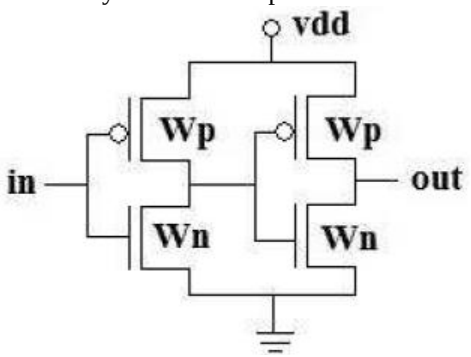


Fig : SIS Comparator

2) Clocked SIS comparator

In clocked switched inverter scheme comparator cascading inverters as a voltage comparator and two set of PMOS and NMOS connected in parallel. The clock pulse is given to the pair of PMOS and NMOS Inverter. Clock is given to the NMOS whereas clockbar is given to PMOS. The two pairs are sized to minimum length and width in nm technology to get reduction in static power dissipation of the overall voltage comparator. Reducing power dissipation is the main performance parameter in Clocked SIS comparator.

3) SIS comparator with sleep transistor

The SIS comparator can be modified with the addition of high threshold PMOS and NMOS near the supply rails. The addition of header & footer reduces the static power dissipation to a great extent due to increased resistance of the high threshold PMOS and NMOS transistors. During the period of no activity the section completely off which is not in use. When any activity is detected, the components are invoked again In this type a local sleep transistor network is used as opposed to global level network, because every comparator is differently sized and so the current through each comparator section is not same.

Another two elements which to be designing are Gain booster and Encoder.

Gain Booster:-

The gain booster is used to increase voltage gain of the output of a comparator so that it provides a full digital output voltage swing, without which the output of the comparator circuit is unable to drive the next stage, it also makes thresholds sharper for comparator outputs and provide full digital output voltage swing. The gain booster block is designed for lowest switching voltage.

Encoder :-

The encoder converts the thermometer code to binary code in two steps .In the first step the thermometer code is converted into one out of n code . The one out of n codes is then converted to binary code d2, d1, d0 by Read only memory (ROM) encoder. The ROM encoder is a common and straight forward approach to encode the one out of n

code to binary bit. The appropriate row m in the ROM is selected by using a row decoder that has the output of comparator m and the inverse of comparator m + 1 as inputs. The output m of the row decoder, connected to memory row m, is high if the output of comparator m is high and the output of comparator m + 1 is low. The row decoder can be realized by, a number of 2-input NAND gates, where one input to each NAND gate is inverted. The main advantage of the ROM decoder approach is its regular structure that is easy to design .

IV. CONCLUSION

In this paper, we are going to design a resistorless analog to digital converter with different comparators using CMOS transistors only. It improves efficiency, reduces chip area and also will have a very low power consumption. Finally analysis of Analog to Digital Converters with different comparators will be made to achieve best efficient of Analog to Digital Converter among others.

REFERENCES

[1] Amol Inamdar, Anubhav Sahu, JieRen, Aniruddha Dayalu, and Deepnarayan Gupta, (2013) "Flash ADC Comparators and Techniques for their Evaluation", IEEE Transactions on Applied Superconductivity, Vol.23, no.3, ISSN No.1051-8223, pp.1-8.

[2] Xiangliang Jin, Zhibi Liu, and Jun Yang, (2013) "New Flash ADC Scheme With Maximal 13 Bit Variable Resolution and Reduced Clipped Noise for High-Performance Imaging Sensor", IEEE Sensors Journal, Vol. 13, no.1, pp. 167-171.

[3] Young-Kyun Cho, Jae-Ho Jung, and Kwang Chun Lee, (2012) "A 9-bit 100-MS/s Flash-SAR ADC without Track-and-Hold Circuits", International Symposium on Wireless Communication Systems (ISWCS), ISSN: 2154-0217, ISBN No. 978-1-4673-0761-1, pp.880-884.

[4] Joyjit Mukhopadhyay and Soumya Pandit, (2012) "Modeling and Design of a Nano Scale CMOS Inverter for Symmetric Switching Characteristics", Hindawi Publishing Corporation VLSI Design, Vol.2012, pp.1-13.

[5] Meghana Kulkarni, V. Sridhar, G.H. Kulkarni,(2010)"4-Bit Flash Analog to Digital Converter Design using CMOS-LTE Comparator", IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) ISBN no. 978-1-4244-7456-1, pp.772-775.

[6] Conor Donovan and Michael P. Flynn, "A Digital 6-bit ADC in 0.25-µm CMOS", IEEE Journal of Solid-State Circuits, Vol. 37, No. 3, March 2002

[7] P.Iyappan, P.Jamuna and S.Vijayasamundiswary, (2009) "Design of Analog to Digital Converter Using CMOS Logic", IEEE International Conference on Advances in Recent Technologies in Communication and Computing, ISBN no. 978-0-7695-3845-7, pp. 74-76.

[8] Yun-ShiangShu, (2012) "A 6b 3GS/s 11mW Fully Dynamic Flash ADC in 40nm CMOS with Reduced Number of Comparators", IEEE Symposium on VLSI Circuits Design, ISBN: 978-1-4673-0848-9, pp. 26-2

[9] Amir Zjajo Jose, Pineda de Gyvez (2011) "Low-Power High Resolution Analog to Digital Converters, Design Test and Calibration" ISBN 978-90-481-9724-8, First edition, Springer NewYork.

[10] Ali Tangel and Kyusun Choi, "The CMOS Inverter as a Comparator in ADC Design",Analog Integrated Circuits and Signal Processing, 39, 147-155, 2004.